evidence that the examiner misidentified these parts; for this reason applicant's conclusory statement that the ferroelectric device level consists of layers 19, 20, 21, and 22 cannot be responded to in a meaningful fashion.

Evidence that the Examiner has misidentified the parts of Kimura's memory device is provided below.

A. Independent claims 39 and 57

Each of independent claims 39 and 57 requires the ferroelectric device level includes at least one ferroelectric capacitor and an overlying ferroelectric isolation layer. With respect to the claimed ferroelectric device level, the Examiner has asserted that Kimura's memory device includes a "ferroelectric device level 14 including at least one ferroelectric capacitor 19-20, and an overlying ferroelectric isolation layer 16."

Contrary to the Examiner's assertion, however, element 14 in Kimura's memory device is a dielectric layer that is aligned only with the lower portions of the two ferroelectric capacitors shown in FIG. 1 of Kimura. No one of ordinary skill in the art at the time of the invention would have considered the dielectric layer 14 to be a "ferroelectric device level 14 including at least one ferroelectric capacitor 19-20," as asserted by the Examiner. Indeed, Kimura clearly shows in FIG. 1 that the ferroelectric capacitors extend above the dielectric layer 14 and therefore, in no sense of the term, could they be considered to be "included" in the dielectric layer 14.

In addition, the Examiner has asserted that layer 16 corresponds to the claimed "overlying isolation layer 16". However, layer 16 does not lie over either of the two capacitors, which are formed of lower electrode 19, capacitor dielectric 20, and plate electrode 21, as shown in FIG. 1. Instead, layer 16 lies under the top portion of plate electrode 21 and adjacent to the top portions of capacitor dielectrics 20 and lower electrodes 19. In addition to not "overlying" the ferroelectric capacitors, layer 16 does not function as a "ferroelectric isolation layer" for the ferroelectric capacitors of Kimura's memory device in accordance with the ordinary and accustomed meaning of the term.

Dielectric layer 22 is the only layer in Kimura's memory device that acts as a ferroelectric isolation layer that overlies at least one ferroelectric capacitor. Accordingly, in order to find in Kimura's memory device a "ferroelectric device level" consistent with claims

39 and 57, one must label the structure formed from the lower electrode 19, the capacitor dielectric 20 and the plate electrode 21 as the claimed "ferroelectric capacitor", and the dielectric layer 22 as the claimed "overlying ferroelectric isolation layer". In this case, however, as shown in FIGS. 1 and 16, there is only one metal level 24 (corresponding to the claimed "first metal level") disposed over the ferroelectric device level (consisting of elements 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23). Therefore, Kimura's memory device does not include an inter-level dielectric level disposed over the first metal level nor does it include a second metal level disposed over the inter-level dielectric level, as recited in each of independent claims 39 and 57.

For at least these reasons, the Examiner's rejection of independent claims 39 and 57 under 35 U.S.C. § 102(e) over Kimura now should be withdrawn.

B. Dependent claims 40, 71, 72, 58, 73, and 74

Claims 40, 71, and 72 incorporate the features of independent claim 39, and claims 58, 73, and 74 incorporate the features of independent claim 57. Therefore, claims 40, 71, 72, 58, 73, and 74 are patentable for at least the same reasons explained above. Claims 71 and 73 also are patentable for the following additional reasons.

Each of claims 71 and 73 recites that between the ferroelectric device level and the transistor isolation layer is *free of any interposing metal level*. The Examiner has asserted that the area between the dielectric layer 14 and the dielectric layer 8 is free of any interposing metal level. Contrary to the Examiner's assertion, however, FIG. 1 clearly shows that Kimura's first embodiment includes a first metal level (consisting of wiring layer 9 and dielectric layer 10) and a second metal level (consisting of second wiring layer 11 and dielectric layer 12), both of which are interposed between the dielectric layer 14 and the dielectric layer 8. For at least this additional reason, claims 71 and 73 are patentable over Kimura.

Applicants presented this explanation for why claims 71 and 73 are patentable over Kimura in the Amendment filed September 3, 2003, yet in the Advisory action dated October 29, 2003, the Examiner conspicuously has failed to address the points raised in this explanation. Applicants request that the Examiner give due consideration of these points.